In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (cancelled).

2. (currently amended) A liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other;

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines;

an array of cells formed in rows and columns, each of the cells being formed near an intersection of one of the gate lines and one of the source lines;

a first transistor of each of the cells disposed at an N-th row and M-th column, N and M being integers, driven by an (N-2)-th gate line;

a second transistor of the each of the cells driven by an N-th gate line; and

~~The device of claim 1, each of the cells further comprising~~ a first capacitor of each of the cells formed between an electrode and the (N-2)-th gate line.

3. (currently amended) The device of claim [[1]]2, each of the cells further comprising a second capacitor formed between an electrode and an (N-1)-th gate line.

4. (cancelled).

5. (currently amended) The device of claim [[4]]3, the first capacitor being charged to a first voltage level in response to a fist state of a signal transmitted on the (N-2)-th gate line, and being discharged to a second voltage level in response to a second state of the signal transmitted on the (N-2)-th gate line.

6. (original) The device of claim 5, an electrical potential at the electrode being pulled up to a third voltage level in response to a first state of a signal transmitted on the (N-1)-th gate line, and being pulled down to the second voltage level in response to a second state of the signal transmitted on the (N-1)-th gate line.

7. (original) The device of claim 6, the first capacitor being charged from the second voltage level to the first voltage level in response to a first state of a signal transmitted on the N-th gate line.

8. (original) A liquid crystal display device comprising:

a plurality of gate lines formed in parallel to each other;

a plurality of source lines formed in parallel to each other and orthogonal to the gate lines; and

an array of cells formed in rows and columns, each of the cells disposed near an intersection of an N-th gate line and an M-th source line, N and M being integers, further comprising:

a first capacitor formed between an electrode and an (N-2)-th gate line; and

a second capacitor formed between the electrode and an (N-1)-th gate line.

9. (original) The device of claim 8 further comprising a first transistor including a gate coupled to the (N-2)-th gate line, and a second transistor including a gate coupled to the N-th gate line.

10. (original) The device of claim 9, the first transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line.

11. (original) The device of claim 9, the second transistor further comprising a first terminal coupled to the electrode, and a second terminal coupled to the M-th source line.

12. (original) The device of claim 8 wherein a signal transmitted on the M-th source line includes a first voltage level and a second voltage level.

13. (original) The device of claim 12, the first capacitor being charged to a third voltage level between the first and second voltage levels after a selection period of the (N-2)-th gate line.

14. (original) The device of claim 12, an electrical potential of the electrode being kept at a third voltage level between the first and second voltage levels after a selection period of the (N-1)-th gate line.

15. (original) The device of claim 12, the first capacitor being charged to the first voltage level after a selection period of the N-th gate line from a third voltage level between the first and second voltage levels.

16. (currently amended) A method of driving a liquid crystal display device comprising:

providing a plurality of gate lines formed in parallel to each other;

providing a plurality of source lines formed in parallel to each other and orthogonal to the gate lines;

forming an array of cells in rows and columns, each of the cells being disposed near an intersection of an N-th gate line and an M-th source line, N and M being integers;

forming a first transistor and a second transistor in the each of the cells;

forming a first capacitor between an electrode and an (N-2)-th gate line in the each of the cells;

driving the first transistor through [[an]]the (N-2)-th gate line; and

driving the second transistor through the N-th gate line.

17. (currently amended) The method of claim 16 further comprising forming ~~a first capacitor between an electrode and the (N-2)-th gate line, and~~ a second capacitor between the electrode and an (N-1)-th gate line in the each of the cells.

18. (original) The method of claim 17 further comprising providing a signal including a first voltage level and a second voltage level from the M-th source line to the first and second transistors.

19. (original) The method of claim 18 further comprising selecting the (N-2)-th gate line, and charging the first capacitor to a third voltage level between the first and second voltage levels after a selection period of the (N-2)-th gate line.

20. (original) The method of claim 18 further comprising selecting the (N-1)-th gate line, and keeping an electrical potential of the electrode at a third voltage level between the first and second voltage levels after a selection period of the (N-1)-th gate line.

21. (original) The method of claim 18 further comprising selecting the N-th gate line, and charging the first capacitor to the first voltage level after a selection

period of the N-th gate line from a third voltage level between the first and second voltage levels.

22. (original) A method of driving a liquid crystal display device comprising:

providing a plurality of gate lines formed in parallel to each other;

providing a plurality of source lines formed in parallel to each other and orthogonal to the gate lines;

forming an array of cells in rows and columns, each of the cells being disposed near an intersection of a corresponding N-th gate line and a corresponding M-th source line, N and M being integers;

providing a signal including a first voltage level and a second voltage level from the M-th source line;

selecting an (N-2)-th gate line;

charging a first capacitor of the each of the cells to a third voltage level between the first and second voltage levels after a selection period of the (N-2)-th gate line;

selecting an (N-1)-th gate line;

keeping an electrical potential of a terminal of the first capacitor at the third voltage level after a selection period of the (N-1)-th gate line;

selecting the N-th gate line; and

charging the first capacitor to the first voltage level after a selection period of the N-th gate line from the third voltage level.

23. (original) The method of claim 22 further comprising forming a first transistor and a second transistor in the each of the cells.

24. (original) The method of claim 23 further comprising driving the first transistor through the (N-2) gate line.

25. (original) The method of claim 23 further comprising driving the second transistor through the N-th gate line.